GATE COMPUTER SCIENCE AND INFORMATION TECHNOLOGY

MULTUPLE SELECT QUESTIONS (MSQ's)

1. Which of the following is/are true about Transmission Control Protocol (TCP):
(a) Application Layer Protocol and uses acknowledgement.
(b) Transport Layer Protocol and checksum for error detection.
(c) Datalink Layer Protocol and acknowledgement.
(d) Transport Layer Protocol and connectionless protocol.

2. User Datagram Protocol (UDP) is used by:
(a) DHCP and Video Streaming.
(b) SMTP and HTTP
(c) DHCP and DNS
(d) DNS and HTTP

3. Which of the following statement is/are correct:
Statement 1: In Internet there is no broadcasting. Any broadcasting done at network layer is converted to broadcasting it at data link layer.
Statement 2: All 0's in Network ID and Host ID part of IP address means host is within the network.
Statement 3: All 1's in Network ID and 0's in Host ID part means subnet mask of the network.
(a) Statement 1 is correct
(b) Statement 1 and 3 are only correct
(c) Statement 1 and 2 are only correct.
(d) Statement 3 is only correct.

4. Which of the following IP addresses cannot be assigned to host for data communication:
(a) 125.10.25.62
(b) 0.0.0.0
(c) 255.255.255.255
(d) 232.45.68.43

5. Which of the following is/are true with respect to IPV4 and IPV6:
(a) There is no requirement of NAT router in IPV6.
(b) IPV6 is a 32-bit protocol.
(c) IPV4 has Header size of more than 60 Bytes.
(d) IPV6 doesn't require DHCP client.

6. Which of the following statement is/are correct:
(a) Ethernet frame include checksum field.
(b) ARP request is normally broadcast, and ARP reply is normally unicast.
(c) Differential Manchester encoding has a transition at the middle of each bit.
(d) IP packet includes a CRC field

7. Which of the following statements is/are true:
(a) ARP is used to find MAC address given an IP address.
(b) ARP is used to find IP address given MAC address
(c) ARP is an application layer protocol

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(d) ARP is a network layer protocol

8. Which of the following are Interior Gateway Protocol
(a) OSPF
(b) OSPF and BGP
(c) BGP
(d) RIP

9. Which of the following are incorrect with respect to Transmission control protocol
(a) TCP has a 4-bit header length field
(b) Tries to Share the bandwidth of bottleneck link among different connections
(c) Connectionless Protocol
(d) TCP has a 224-bit header length field

10. In classless inter domain routing which of the following statement is/are true?
(a) All the IP addresses in a block should be contiguous.
(b) The number of IP addresses in a block should be a power of 2.
(c) First IP address in the block should be divisible by size of block.
(d) If IP address the least significant part should always start with zeroes in Host Id, then we can use it as Block Id part.

11. There are three process P1, P2, P3 using shortest remaining time first scheduling:

P. No.	Arrival Time	CPU time	I/O time	CPU time
1	0	1	2	2
2	1	2	4	5
3	2	3	6	8

Note: (i) Process first spends CPU time followed by I/O time and followed by CPU time again.
(ii) I/O of the processes can be overlapped as much as possible.
(a) The completion time of the process P1 and P2 are 5 and 13.
(b) The completion time of the process P2 and P3 are 13 and 22.
(c) The completion time of the process P1 and P3 are 7 and 18.
(d) The completion time of the process P2 and P3 are 11 and 18.

12. There are three process P1, P2, P3 using shortest remaining time first scheduling:

P. No.	Arrival Time	I/o time	CPU time	I/O time
1	0	1	2	2
2	1	2	4	5
3	2	3	6	8

Note: (i) Process first spends I/O time followed by CPU time and followed by I/O again.
(ii) I/O of the processes can be overlapped as much as possible.
(a) The completion time of the process P1 and P2 are 15 and 53.
(b) The completion time of the process P2 and P3 are 50 and 94.
(c) The completion time of the process P1 and P3 are 20 and 94.
(d) The completion time of the process P2 and P3 are 53 and 108.

13. In which of the following scheduling algorithm starvation is possible?
(a) Non-pre-emptive SJF and Pre-emptive priority scheduling
(b) Non-pre-emptive priority scheduling and multilevel queue scheduling algorithm

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(c) Round robin and FCFS prescheduling
(d) Round robin non-pre-emptive scheduling and FCFS non-pre-emptive scheduling

14. Mutual exclusion and progress is/are satisfied in which of the following algorithms.
(a) Lock variables
(b) Strict alteration
(c) Peterson algorithm
(d) Test and Set Instruction

15. Benefits of using threads in operating systems is/are:
(a) Faster context switching and Resource sharing
(b) Improve Responsiveness and Economical
(c) Effective utilization of multiprocessor systems and Enhanced throughput of the system
(d) Good scalability

16. Thrashing in page replacement policy is/are caused due to
(a) High Degree of multiprogramming
(b) Lack of frames in main memory
(c) IIigh number of frames in main memory
(d) Low Degree of multiprogramming

17. Consider the system with the below statistics observation
(i) CPU utilization -10%
(ii) Paging disk- 90%
Which of the below factors will improve the CPU utilization?
(a) Install bigger disk
(b) Decrease page size
(c) Decrease degree of multiprogramming
(d) Install more main memory

18. Which of the following statements are true:
(a) Every finite language is regular
(b) Every regular language is finite
(c) Every infinite language is non-regular
(d) A language L is regular if and only if there is a regular expression for L

19. Which of the following is/are regular sets?
(a) $\{a^n b^{2m} \mid n \geq 0, m \geq 0\}$
(b) $\{a^{(n^2)} \mid n \leq 100\}$
(c) $\{a^m b^n \mid \text{GCD}(m,n) = 1\}$
(d) $\{a^n b^m \mid n = 2m\}$

20. Which of the following languages is/are closed under intersection and complement.
(a) Regular languages
(b) Context free languages
(c) Regular and recursive languages
(d) Recursive and recursive enumerable languages

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21. Which of the following languages is/are context free.

(a) $\{a^n b^n c^n \mid n, m \geq 0\}$

(b) $\{a^n b^m c^{n+m} \mid n, m \geq 0\}$

(c) $\{a^n b^{n+m} c^m \mid n, m \geq 0\}$

(d) $\{a^n b^m c^n d^m \mid n, m \geq 0\}$

22. Which of the following statements is/are correct.
(a) Every subset of countable set is countable
(b) Countable infinite union of countable set is countable
(c) Every language is always countable
(d) If S is countable infinite then 2^S is uncountable infinite

23. Which of the following problems is/are undecidable problems?
(a) Post-correspondence problem of turning machine
(b) 3-SAT problem
(c) k-colourability problem
(d) Min-Cut problem

24. Recursive languages are:
(a) a proper superset of context free languages.
(b) always recognizable by pushdown automata
(c) also called type-0 languages
(d) recognizable by Turing machines

25. A core of processor chip consists of:
(a) ALU
(b) Instruction logic
(c) Load/store logic
(d) L1 data cache

26. Which of the following will cause internal interrupt to CPU:
(a) Stack overflow
(b) Attempt to divide by zero
(c) I/O device finished transfer of data
(d) Power failure

27. What are the components of a memory management unit:
(a) A facility for dynamic storage relocation
(b) Provision for preventing users for sharing programs stored in memory by different users
(c) Protection of information against unauthorized access
(d) Provision for users for changing operating system functions

28. Which of the following steps are followed by HIS during synthesis:
(a) Data model generation
(b) Data flow analysis
(c) Scheduling and allocation
(d) Data path optimization

29. Which of the following statements are correct:
(a) A pseudo instruction is a machine instruction.

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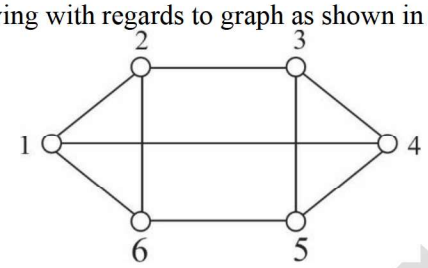
(b) A pseudo instruction is an instruction to the assembler.
(c) The ORG (origin) is an example of pseudo instruction.
(d) It is not possible to use ORG more than once in a program.

30. Which of the following are the advantages of packet switching:
(a) Greater link efficiency than circuit switching
(b) Connections are not blocked when traffic congestion occurs
(c) Direct channel established between transmitter and receiver
(d) No time is taken to establish connection

31. Which of the following with regards to graph as shown in the following figure are correct:



(a) Regular graph
(b) Connected graph
(c) Complete graph
(d) Non-regular graph

32. Which of the following statements regarding the functions of an operating system in a computer are correct:
(a) It controls hardware access.
(b) It manages files and folders.
(c) It provides a user interface.
(d) It manages applications.

33. Which of the following statements regarding database normal forms are correct:
(a) Any relation with two attributes is BCNF.
(b) Lossless, dependency-preserving decomposition into BCNF is always possible.
(c) Lossless, dependency-preserving decomposition into 3NF is not possible.
(d) BCNF is stricter than 3NF.

34. The 8259A Programmable Interrupt Controller can:
(a) manage eight interrupts
(b) vector an interrupt request anywhere in the memory map
(c) have 8-bit or 16-bit interval between interrupt vector locations
(d) be initialized with operational command words

35. Which of the following are typical elements of machine instructions:
(a) Operation code
(b) Source operand reference
(c) Result operand reference
(d) Next instruction reference

36. Which of the following statements are correct:
(a) DRAM offers reduced power consumption.
(b) An associative memory is cheaper than RAM.
(c) The fastest and most flexible cache organization uses content addressable memory.

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(d) The address generated by a segmented program is called a physical address.

37. With reference to 8085 microprocessor, which of the following statements are correct:
(a) The DAD instruction adds the contents of the specified register pair to the contents of the DL register pair.
(b) The program counter is an instruction pointer.
(c) Whenever an instruction uses the HL pointer, the addressing is called indirect addressing.
(d) HL register pair is also called memory pointer.

38. On the 8085, which of the following machine cycles are not used in the CALL instruction:
(a) Instruction fetch
(b) I/O
(c) Memory Read
(d) Memory Write

39. The stack pointer will be affected by instructions
(a) PUSH PSW
(b) CALL ADDR
(c) XTHL
(d) RST n

40. Which of the following statements for a DRAM are correct:
(a) Bit is stored as a charge.
(b) It is made of MOS transistors.
(c) Speed of DRAM is faster than processors.
(d) Each memory cell requires six transistors.

41. Which of the following are 8085 software interrupts:
(a) INTR
(b) RST 6
(c) RST 7.5
(d) RST0

42. Which of the following statements about CMOS are correct:
(a) CMOS logic inverter has maximum signal swing of 0 V to V_{DD}.
(b) The output signal swing is independent of exact value of aspect ratio and other device parameters.
(c) It is a fast switching device with wide noise margins.
(d) It has zero input resistance and infinite output resistance.

43. Which of the following are universal gates:
(a) AND
(b) NAND
(c) NOR
(d) NOT

44. The logic function:

$$\text{Out} = ab + bc + ca$$

Defines:
(a) The output of a 3-inputs XOR gate
(b) The output of a 3-inputs majority gate
(c) The sum output of a full adder
(d) The carry output of a full adder

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45. Which of the following are source codes:
(a) Hamming code
(b) Huffman code
(c) Shannon-Fano code
(d) Convolutional code

46. Sorting is useful for:
(a) Report generation
(b) Making searching easier and efficient
(c) Responding to queries easily
(d) Minimizing the storage needed

47. Which of these are included in the present definition of computer architecture to design a full computer system:
(a) Compilers
(b) Design
(c) Evaluation
(d) Instruction set architecture

48. The interfacing of assembly language routines with some high level language, one must address which of the following are correct:
(a) How is the subroutine invoked?
(b) How are parameters passed?
(c) How are values returned?
(d) How many parameters are passed?

49. The parallel computers are divided into which of the following architectural configuration:
(a)Array processors
(b) Data processors
(c) Multi processor systems
(d) Pipeline computers

50. A good line code should have which of the following are correct:
(a) Favorable pad
(b) Low inter symbol interference
(c) Adequate timing content
(d) Transparency

51. On the 8085, which of the following machine cycles are used in the CALL instruction:
(a) Instruction Fetch
(b) I/O
(c) Memory Read
(d) Memory Write

52. What are the ultimate purposes of minimising logic expressions:
(a) To get a small size expression.
(b) To reduce the number of variables in the given expression.
(c) To implement the function of the logic expression with least hardware.
(d) To reduce the expression for making it feasible for hardware implementation.

53. Which of the following circuits come under the class of sequential logic circuits:

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(a) Full adder
(b) Full subtractor
(c) *JK* flip-flop
(d) Counter

54. Which of the following statements regarding registers and latches are correct:
(a) Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs.
(b) Registers are temporary storage devices whereas latches are not.
(c) A latch employs cross-coupled feedback connections.
(d) A register stores a binary word whereas a latch does not.

55. Which of the following capabilities are available in a Universal Shift Register:
(a) Shift left
(b) Shift right
(c) Parallel load
(d) Serial add

56. Which of the following measurements can be done using a counter are correct:
(a) Pulse duration
(b) Interval between two pulses
(c) Amplitude of the pulse
(d) Rise time of a pulse

57. With reference to C programming language, which of the following statements are correct:
(a) An identifier may start with an underscore.
(b) An identifier may end with an underscore.
(c) IF is a valid identifier.
(d) The number of significant characters in an identifier is implementation dependent.

58. Which of the following statements are correct:
(a) Internal sorting is used if the number of items to be sorted is very large.
(b) External sorting is used if the number of items to be sorted is very large.
(c) External sorting needs auxiliary storage.
(d) Internal sorting needs auxiliary storage.

59. Which of the following statements are correct:
(a) Bus is a group of wires carrying information.
(b) Bus is needed to achieve reasonable speed of operation.
(c) Bus can carry data or address.
(d) A bus can be shared by more than one device.

60. The 8259 A programmable interrupt controller can
(a) Manage eight interrupts
(b) Vector an interrupt request anywhere in memory map
(c) Have 8-bit of 16 bit interval between interrupt vector locations
(d) Initialized with operational command words (OCW's)

61. Which of the following are the objectives of a data acquisition system?
(a) It must acquire necessary data at correct speed and time.

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(b) It must collect and store data.
(c) There should be provision for real-time data display.
(d) There should be provision for stored data display on request.

62. Arithmetic Logic Unit (ALU)
(a) Performs arithmetic operations
(b) Performs comparisons
(c) Communicates with I/O devices
(d) Keeps watch on the system

63. Which of the following expressions are equivalents of the expression $Y = A \oplus B \oplus C \oplus D$:
(a) $Y = f(A, B, C, D) = \sum(1, 2, 4, 7, 8, 11, 13, 14)$
(b) $Y = f(A, B, C, D) = \sum(3, 5, 7, 10, 11, 12, 13, 14)$
(c) $Y = f(A, B, C, D) = \Pi(0, 3, 5, 6, 9, 10, 12, 15)$
(d) $Y = f(A, B, C, D) = \Pi(0, 1, 2, 4, 6, 8, 9, 15)$

64. Which of the following 8-bit registers of 8085 μP can be paired together to make a 16-bit register?
(a) Accumulator and flag register
(b) B and C registers
(c) D and E registers
(d) H and L registers

65. Which of the following options is/are correct:
(a) Race-around condition occurs in a *JK* flip-flop when the inputs are 1, 1
(b) A flip-flop is used to store one bit of information
(c) A transparent latch consists of *D* type flip-flops
(d) Master-slave configuration is used in a flip-flop to store two bits of information

66. If a, b, c are 3-input variables, then Boolean function $y = ab + bc + ca$ represents
(a) A 3-input majority gate
(b) A 3-input minority gate
(c) Carry output of a full adder
(d) Product circuit for a, b and c

67. Which of the following instructions are machine control instructions:
(a) LOCK
(b) STD
(c) HLT
(d) CLI

68. If the interrupt for 8085 microprocessor is to be vectored to any memory location then which of the following interrupts is/are correct:
(a) INTR
(b) RST 5.5
(c) RST 6.5
(d) RST 7.5

69. Which of the following options is/are correct:
(a) Semiconductor memories are organized as linear array of memory locations

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(b) To address a memory location out of N memory locations, at least log N bits of address are required
(c) 8086 can address 1,048,576 addresses
(d) Memory for an 8086 is set up as two banks to make it possible to read or write a word with one machine cycle

70. Which of the following statements are correct about SRAM?
(a) It provides faster access as compared to DRAM.
(b) It is cheaper than DRAM.
(c) It is more expensive than DRAM.
(d) It has higher bit density than DRAM.

71. The memory management function of virtual memory includes
(a) Space allocation
(b) Program relocation
(c) Program execution
(d) Code sharing

72. Which of the following stacks are not used in 8085 microprocessors:
(a) FIFO
(b) FILO
(c) LIFO
(d) LILO

73. Counting Sort is best suited for:
(a) Data disbursed in short range
(b) Data disbursed in long range
(c) Number of inputs quite larger than the range
(d) Number of inputs quite smaller than the range

74. Which of following sorting algorithm(s) has/have linear complexity in best case
(a) Quick Sort
(b) Bucket Sort
(c) Radix Sort
(d) Insertion Sort

75. What are the Factors upon which sorting algorithm is dependent:
(a) No. of items to be sorted
(b) Extent to which the items are already sorted
(c) Possible restriction on items value
(d) Kind of storage device to be used – main memory, disks, or tape

76. Which algorithm design strateg(y)(ies) is/are preferable for optimization problems:
(a) Greedy Method
(b) Dynamic Programming
(c)Divide and Conquer
(d) Incremental Approach

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77. Which of following problem(s) may be solved using Dynamic Programming algorithm design technique:
(a) Fractional Knapsack
(b) 0/1-Knapsack
(c) Matrix Chain Multiplication
(d) Starssen's Matrix Multiplication

78. If a graph has negative edge then which algorithm should not be applied for Single Source Shortest Path:
(a) Dijkastra's
(b) Kruskal's
(c) Prim's
(d) Bellman-Ford

79. If a graph has negative cycle then which of following statement(s) is/are true with respect to Single Source Shortest Path Problem:
(a) There are no SSSP exits if a graph has negative cycle.
(b) Bellman-Ford Algorithm for SSSP give the answer that there does not exists any solution for this problem instance.
(c) There are infinitely many solutions for this problem.
(d) Unique solution can be found out by Floyd-Warshal's Algorithm

80. Which of the followings is/are the algorithm(s) to find the Minimum Spanning Tree of a graph?
(a) Prims's
(b) Flloyd-Warshal's
(c) Dijkastra's
(d) Kruskal's

81. Floyd-Warshall Algorithm for all pair shortest path problem is not an example of which algorithm design technique:
(a) Incremental Approach
(b) Divide & Conquer
(c) Dynamic Programming
(d) Greedy Method

82. Which of the statement(s) is/are true with respect to All pair shortest path problem:
(a) Given a directed graph $G = (V, E)$, weight function $w : E \rightarrow \boldsymbol{R}$, $|\boldsymbol{V}| = \boldsymbol{n}$.
(b) There is unique vertex called starting vertex
(c) Goal: create an $n \times n$ matrix of shortest-path distances $\delta(u, v)$.
(d) There is an unique vertex called destination vertex.

83. Which of the followings algorithm(s) have $O(E\log V)$ time complexity, where E is number of edges and V is the number of vertices in a graph?
(a) Prims's
(b) Flloyd-Warshal's
(c) Dijkastra's
(d) Kruskal's

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84. Consider the following statements with queries.

S1: [Select * from R_1, R_2] is equal to $[R_1 \times R_2]$.

S2: [R_1 θ __ R_2] is equal is equal to $[R_1 \times R_2]$.

Identify the valid statements?

(a) S1
(b) S2
(c) S1 or S2
(d) None of the above

85. Given the basic ER and relational models, which of the following is INCORRECT?

(a) An attribute of an entity can have more than one value
(b) An attribute of an entity can be composite.
(c) An attribute set is denoted by rectangle.
(d) An attribute can have more than one value.

86. Consider the following two statements about database transaction schedules:

I. Strict two-phase locking protocol generates conflict serializable schedules that are also recoverable.
II. Timestamp-ordering concurrency control protocol with Thomas Write Rule can generate view serializable schedules that are not conflict serializable.
III. Recoverable schedules are also conflict serializable.

Which of the above statements is/are TRUE?

(a) Statement 1 is correct.
(b) Statement 2 is correct.
(c) Statement 3 is correct.
(d) All of the above statements are correct.

87. Which of the following concurrency control protocols do not ensure both conflict serializability and freedom from deadlock?

(a) 2-phase locking
(b) Time-stamp ordering
(c) Simple locking (Shared and Exclusive) protocols
(d) 1-phase locking

88. Given the following two statements:

S1: Every table with two single-valued attributes is in 1NF,2NF,3NF and BCNF
S2: AB→C, D→E, E→C is a minimal cover for the set of functional dependencies.

Which one of the following is CORRECT?

(a) S1 is true
(b) S2 is false
(c) S1 is false
(d) S2 is true

89. Relation R has eight attributes ABCDEFGH.

Fields of R contain only atomic values.

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F = {CH→G, A→BC, B→CFH, E→A, F→EG} set of functional dependencies (FDs) so that F+ is exactly the set of FDs that hold for R.
The relation R is in
(a) 1st Normal Form
(b) 2nd Normal Form
(c) Not in 2NF
(d) BCNF

90. Which one of the following statements is NOT correct about the B+ tree data structure used for creating an index of a relational database table?
(a) B+ tree root node stores the record pointers.
(b) B+ tree is a height balanced tree.
(c) Non-leaf nodes have pointers to data records.
(d) Key values are kept in sorted order

91. Consider the following two phase locking protocol.
Suppose a transaction T accesses (for read or write operations), a certain set of objects $\{O_1,...,O_k\}$. This is done in the following manner:
Step 1. T acquires exclusive locks to $O_1,...,O_k$ in increasing order of their addresses.
Step 2. The required operations are performed.
Step 3. All locks are released.
This protocol will
(a) Guarantees Serializability
(b) Guarantees Serializability but not Deadlock Freedom
(c) Deadlock Freedom but not Guarantees Serializability
(d) Deadlock Freedom

92. Consider the following partial Schedule S involving two transactions $T1$ and $T2$. Only the read and the write operations have been shown. The read operation on data item P is denoted by read(P) and the write operation on data item P is denoted by write(P).
$R1(A)$ $W1(A)$ $R2(C)$ $W2(C)$ $R2(B)$ $W2(B)$ $R2(A)$ COMMIT $R1(B)$.
Suppose that the transaction $T1$ fails immediately after time instance 9. Which one of the following statements is correct?
(a) $T2$ must be aborted and then both transactions must be re-started to ensure transaction atomicity.
(b) Only $T2$ must be aborted and then re-started to ensure transaction atomicity.
(c) Schedule S is non-recoverable
(d) Schedule S cannot ensure transaction atomicity.

93. Consider the transactions $T1$, $T2$, and $T3$ and the schedules $S1$ and $S2$ given below.
$T1$: $r1$ (X); $r1$ (Z); $w1$ (X); $w1$ (Z)
$T2$: $r2$ (X); $r2$ (Z); $w2$ (Z)
$T3$: $r3$ (X); $r3$ (X); $w3$ (Y)
$S1$: $r1(X)$; $r3(Y)$; $r3(X)$; $r2(Y)$; $r2(Z)$; $w3(Y)$; $w2(Z)$; $r1(Z)$; $w1(X)$; $w1(Z)$
$S2$: $r1(X)$; $r3(Y)$; $r2(Y)$; $r3(X)$; $r1(Z)$; $r2(Z)$; $w3(Y)$; $w1(X)$; $w2(Z)$; $w1(Z)$
Which one of the following statements about the schedules is TRUE?
(a) Only $S1$ is conflict Serializable
(b) $S1$ is view Serializable

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(c) $S2$ is view Serializable
(d) Only $S2$ is conflict Serializable

94. Which of the following is/are correct to initialise an array in C
(a) `Int a[3]={2,3,4};`
(b) `Int a[3]=[1,2,4];`
(c) `Int a[]={1,2,3};`
(d) `Int a[3]=(1,2,3);`

95. Which of the following is/are correct about the recursion:
(a) Recursion cannot solve problem without base case
(b) Recursion take less time than the iteration.
(c) Recursion required more memory than the iteration.
(d) Iteration required more memory than the recursion

96. Consider a linked list of n nodes and pointer is pointing to first node. Which of the following is/are true?
(a) Time require to insert node at second position is O(1).
(b) Time require to insert node at end is $O(n\log n)$
(c) Time require to insert node at end is $O(n)$
(d) Time required to search a node is $O(n)$.

97. Which of the following statements are correct
(a) Stack data structure is used to implement the recursion algorithm.
(b) Queue data structure is used to check weather an expression contains balance parenthesis.
(c) Stack data structure is used to evaluate the postfix expression.
(d) Stack data structure is used for DFS in graph.

98. Which of the following statements are true about queue
(a) In queue Rear is used for deletion and Front is used for insertion.
(b) Queue is linear data structure which work on the principle on FIFO.
(c) For BFS in graph queue is use.
(d) For DFS in graph queue is used.

99. $O(n\log n)$ is the worst-case complexity for:
(a) Merge sort
(b) Quick sort
(c) Heap sort
(d) Selection sort

100. Which of the following is/are true about a binary tree with n nodes and h height
(a) Maximum height of the tree is $n - 2$.
(b) Minimum height of the tree is $\log_2 n$.
(c) Minimum number of nodes is $h + 1$.
(d) Maximum number of nodes is $2h + 1$.

101. Which of the following statements is/are correct about graph.
(a) In a complete graph with n vertices has $(n*(n - 1))/2$ number of edges.
(b) A graph may contain many vertices and no edges.
(c) A graph with all vertices having equal degree is called regular graph
(d) A graph with all vertices having equal degree is called planer graph

102. Consider the following statements about the heap

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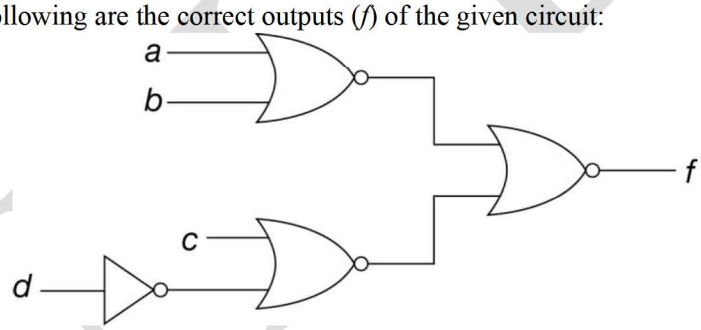
(a) In max heap largest element is at root node
(b) Heap can be used as a priority queue
(c) In Min heap smallest element is at root node.
(d) Smallest element can be find from max heap in O(1).

103. Which of the following flags are present in 8085 microprocessors:
(a) Sign flag
(b) Trap flag
(c) Parity flag
(d) Auxiliary flag

104. In 8085 microprocessor, data-bus and address-bus are multiplexed in order not to
(a) Increase the speed of microprocessor
(b) Reduce the number of pins
(c) connect more peripheral chips
(d) Increase the number of pins

105. For 16-bit address-bus, if an 8K RAM chip is selected when, A13, A14, and A15 address bits are all one, then what are ranges of the memory address?
(a) E000H – EEEEH
(b) F000H – FF00H
(c) FF00H – FFFFH
(d) C000H – DFFFH

106. Which of the following are the correct outputs (*f*) of the given circuit:



(a) $f = (a+b)(c+\overline{d})$
(b) $f = \overline{(a+b)}\,\overline{(c+\overline{d})}$
(c) $f = ac + a\overline{d} + bc + b\overline{d}$
(d) $f = \overline{\overline{\overline{(a+b)} + \overline{(c+\overline{d})}}}$

107. In an instruction of 8085 microprocessor, how many bytes are present?
(a) One
(b) Two
(c) Three
(d) eight

108. If X_1 and X_2 are the inputs to the circuit as shown in the following figure, then what are the output Q?

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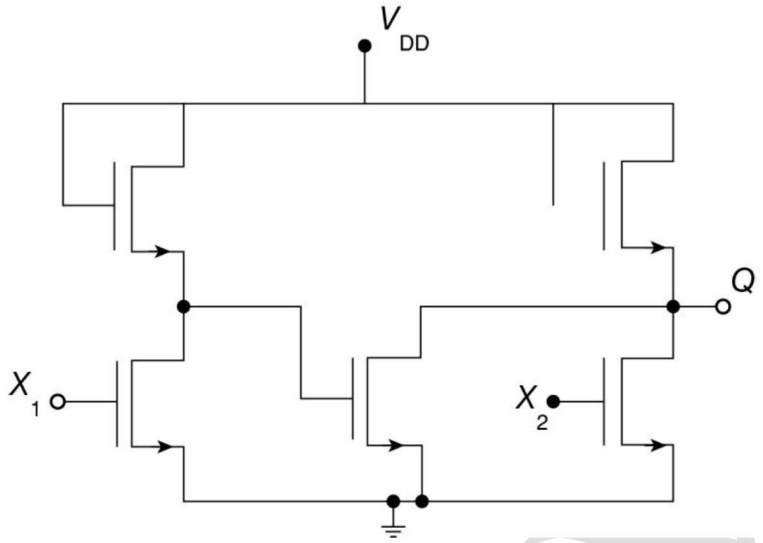

(a) $Q = X_1\bar{X}_2$

(b) $Q = \overline{(\bar{X}_1 X_2)}$

(c) $Q = \overline{(\bar{X}_1 + X_2)}$

(d) $Q = X_1 + \bar{X}_2$

109. Which of the following are correct match of instruction code and addressing mode:
(a) JUMP 2021 H – Immediate addressing mode
(b) LDAX B – Indirect Resister addressing mode
(c) IN 10H – Direct addressing mode
(d) RLC – Implicit addressing mode

110. Which of the following addressing techniques are used in 8085 microprocessors:
(a) Register
(b) Immediate
(c) Register indirect
(d) Relative

111. Which of the following statements are true:
(a) Delayed control transfer involves starting the execution of the instruction after a branch or control instruction, regardless of whether the branch is taken.
(b) One way to implement branch prediction is to store the result of a branch condition in a branch target buffer to help guide instruction prefetching if the branch is encountered again later.
(c) If a multi-cycle, pipelined processor has N pipeline stages, then structural hazards can be avoided completely if at least N registers are available.
(d) If a multi-cycle, pipelined processor has N pipeline stages, then structural hazards can be avoided completely if at least $N/2$ registers are available.

112. A certain hard drive rotates at 6000 rpm. It has 1 KB per sector and averages 128 sectors per track. Which of the following statements are true:
(a) The average latency of the drive is under 6 milliseconds.
(b) The burst data rate of the drive is over 10 MB/s.
(c) The average capacity per track is over 1 MB.

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(d) The burst data rate of the drive is over 1 MB/s.

113. The designers of a computer must select a cache system. They have two options.
Design #1 uses a direct-mapped cache containing 2 words per cache line. It would have an instruction miss rate of 3% and a data miss rate of 8%.
Design #2 uses a 2-way set associative cache containing 8 words per cache line. It would have an instruction miss rate of 1% and a data miss rate of 4%.
For each design, there will be approximately 0.5 data references on average per instruction. The cache miss penalty in clock cycles is 8 + cache line size in words; for example, the penalty with 1-word cache lines would be 8 + 1 = 9 clock cycles.
Let D_1 be cycles wasted by Design #1 on cache miss penalties (per instruction) and D_2 be cycles wasted by Design #2 on cache miss penalties (per instruction).
On average, how many clock cycles will be wasted by each on cache miss penalties?
(a) $D_1 = 0.70$
(b) $D_1 = 1.10$
(c) $D_2 = 0.48$
(d) $D_2 = 0.40$

114. A binary single-precision floating point number contains the sequence of bits 10001111100000000001000000000000. Information is stored in the following left-to-right order: sign bit, exponent (bias −127), and mantissa (with an implied unit bit).
Which of the following representations in decimal are not equivalent:
(a) $231 * (1 + 2 - 12)$
(b) $-1 * 231 * (1 + 2 - 12)$
(c) $-1 * 2 - 65 * (1 + 2 - 10)$
(d) $-1 * 2 - 96 * (1 + 2 - 11)$

115. Consider the following two designs for a little cache.
Design #1 is a direct-mapped cache of 8 1-word cache lines. The miss penalty is 8 clock cycles.
Design #2 can store the same total number of items as Design #1, but it is a two-way associative cache of 1-word cache lines. Least-recently-used is utilized to determine which items should be removed from the cache. The miss penalty is 10 clock cycles. Suppose that the following eight memory references arrive.
Memory References: 0, 3, 14, 11, 4, 11, 8, 0
How much time will these designs spend on cache miss penalties, assuming that the caches start empty?
(a) Design #1 spends 56 cycles
(b) Design #1 spends 64 cycles
(c) Design #2 spends 70 cycles
(d) Design #2 spends 60 cycles

116. The designers of a cache system need to reduce the number of cache misses that occur in a certain group of programs. Which of the following statements is/are true?
(a) If compulsory misses are most common, then the designers should consider increasing the cache line size to take better advantage of locality.
(b) If capacity misses are most common, then the designers should consider increasing the total cache size so it can contain more lines.
(c) If conflict misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.

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(d) If capacity misses are most uncommon, then the designers should consider decreasing the total cache size so it can contain more lines.

117. Consider a CPU having 33 registers and uses 14 addressing modes. RAM is 32K x 48. The instruction has the operation code (op- code), register operand and a memory address operand fields. Which of the following is/are true?
(a) Length data lines is 48 bits
(b) Maximum size of the register field is 5 bits
(c) Memory Address field requires 15 bits
(d) Maximum size of the op-code is 23 bits

ANSWER KEY

1.	(b, d)	**2.**	(a, c)	**3.**	(a, b)	**4.**	(b, c)	**5.**	(a, d)
6.	(b, c)	**7.**	(a, d)	**8.**	(a, d)	**9.**	(a, b)	**10.**	(a, b, c, d)
11.	(a, b)	**12.**	(b, c)	**13.**	(a, b, d)	**14.**	(c, d)	**15.**	(a, b, c, d)
16.	(a, b)	**17.**	(c, d)	**18.**	(a, d)	**19.**	(a, d)	**20.**	(a, c)
21.	(b, c)	**22.**	(a, b, c, d)	**23.**	(a, b, c)	**24.**	(a, c, d)	**25.**	(a, b, c, d)
26.	(a, b)	**27.**	(a, c)	**28.**	(a, b, c, d)	**29.**	(b, c)	**30.**	(a, b)
31.	(a, b)	**32.**	(a, b, c, d)	**33.**	(a, c, d)	**34.**	(a, b, d)	**35.**	(a, b, c)
36.	(a, c)	**37.**	(b, c, d)	**38.**	(a, c, d)	**39.**	(a, b, d)	**40.**	(a, b)
41.	(b, d)	**42.**	(a, b, c)	**43.**	(b, c)	**44.**	(b, d)	**45.**	(b, c)
46.	(a, b, c, d)	**47.**	(b, c, d)	**48.**	(a, b, c)	**49.**	(a, c, d)	**50.**	(a, b, c, d)
51.	(a, c, d)	**52.**	(c, d)	**53.**	(c, d)	**54.**	(a, c)	**55.**	(a, b, c)
56.	(a, b)	**57.**	(a, b, c, d)	**58.**	(b, c)	**59.**	(a, b, c, d)	**60.**	(a, b)
61.	(a, b, c, d)	**62.**	(a, b, c)	**63.**	(a, c)	**64.**	(b, c, d)	**65.**	(a, b, c)
66.	(a, c)	**67.**	(a, c)	**68.**	(b, c, d)	**69.**	(a, b, c, d)	**70.**	(a, c)
71.	(a, b, d)	**72.**	(a, b, d)	**73.**	(a, c)	**74.**	(b, c, d)	**75.**	(a, b, c, d)
76.	(a, b)	**77.**	(b, c)	**78.**	(a, b, c)	**79.**	(a, b, c)	**80.**	(a, d)
81.	(a, b, d)	**82.**	(b, d)	**83.**	(a, d)	**84.**	(a, b)	**85.**	(c, d)
86.	(a, b)	**87.**	(b, c)	**88.**	(a, b)	**89.**	(a, c)	**90.**	(a, c)
91.	(a, d)	**92.**	(c, d)	**93.**	(a, b)	**94.**	(a, c)	**95.**	(a, c)
96.	(a, c, d)	**97.**	(a, c)	**98.**	(b, c)	**99.**	(a, c)	**100.**	(b, c)
101.	(a, b, c)	**102.**	(a, b, c)	**103.**	(a, c, d)	**104.**	(a, c, d)	**105.**	(a, b, c)
106.	(a, c, d)	**107.**	(a, b, c)	**108.**	(a, c)	**109.**	(a, b, c, d)	**110.**	(a, b, c)
111.	(a, b, c)	**112.**	(a, b)	**113.**	(a, c)	**114.**	(a, b, c)	**115.**	(a, c)
116.	(a, b, c)	**117.**	(a, b, d)						

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