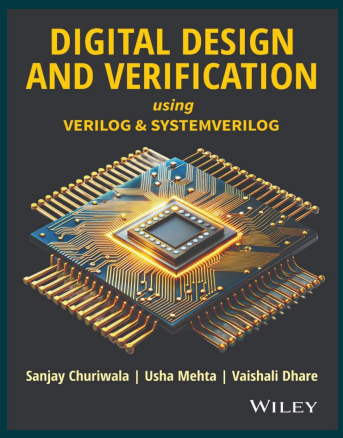
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Digital Design and Verification using Verilog and SystemVerilog

By Sanjay Churiwala, Usha Mehta, Vaishali Dhare

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Description

Digital Design and Verification using Verilog and SystemVerilog is an essential guide for students and early career professionals aiming to master the intricacies of digital design and verification. Authored by industry experts and academics, this book combines practical insights from the field with foundational teaching principles, making it a comprehensive resource for learning and applying Verilog and SystemVerilog.

About the Author

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Sanjay Churiwala holds a B.Tech in Electronics and Electrical Communications Engineering from IIT Kharagpur. With over 30 years of experience in VLSI front-end design methodologies and Electronic Design Automation, he has extensively worked on Verilog-based designs in various roles, including Applications Engineering, Design and Verification Lead, and Tool Development and Verification. He holds several international patents and has authored numerous technical books on VLSI and related fields. Currently, he serves as the Corporate Vice President at AMD's Hyderabad office. Sanjay is also a regular guest lecturer on VLSI topics at various academic institutions.

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With over 20 years of teaching experience, she has guided more than 30 MTech and BTech projects and conducted various seminars and workshops. She has published over forty papers in journals and conference proceedings and is currently guiding two research scholars. She has also undertaken consultancy and research projects. Her areas of interest include Hardware Description Languages, Testing and Verification of VLSI Design, Quantum-dot Cellular Automata, Applied Algorithms for VLSI CAD, and Reversible Logic.

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